IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table; and

oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm.

2. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

3-4. (Canceled)

5. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

6. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

7. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

8. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

9. (Previously Presented) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table; and

oxidizing the metal layer using a krypton(Kr)/oxygen (O_2) mixed plasma process to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm.

10. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

11-12. (Canceled)

13. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

14. (Previously Presented) A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm; and

coupling a gate to the metal oxide layer.

15. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

16-17. (Canceled)

18. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

19. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

20. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

21. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

22. (Previously Presented) A method of forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

24-25. (Canceled)

26. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

27. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

28. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

29. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

30. (Previously Presented) A method of forming an information handling system, comprising:

forming a processor;

forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

31. (Original) The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

32-33. (Canceled)

34. (Original) The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

35. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

36. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

37. (Original) The method of claim 30, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

38-50. (Canceled)

51. (Previously Presented) A transistor formed by the process, comprising:

forming a body region coupled between a first source/drain region and a second source/drain region;

evaporation depositing a substantially amorphous and substantially single element metal layer directly contacting the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm; and

coupling a gate to the metal oxide layer.

52. (Original) The transistor of claim 51, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

53. (Canceled)

54. (Original) The method of claim 51, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

55. (Previously Presented) A method of forming a gate oxide on a transistor body region, comprising:

electron beam evaporation depositing a substantially amorphous and substantially pure zirconium layer directly contacting the body region; and

oxidizing the zirconium layer to form a metal oxide layer directly contacting the body region, wherein the metal oxide layer has a smooth surface with a surface roughness variation of 0.6 nm.

56. (Previously Presented) The method of claim 55, wherein oxidizing the zirconium layer includes oxidizing a zirconium layer to form an oxide with a conduction band offset in a range of approximately 5.16 eV to 7.8 eV.

57-61. (Canceled)

62. (Original) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a substantially amorphous and substantially single element, group IVB metal layer directly contacting the body region using electron beam evaporation while maintaining the smooth surface of the body region; and

oxidizing the metal layer to form a metal oxide layer directly contacting the body region at the smooth surface.